For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art, and therefore request that the pending rejections be withdrawn.

II. The Objection To The Drawings And Specification

The specification and drawings were objected to for failing to describe and illustrate a gate and an impurity diffusion as recited in claim 4. While Applicants respectfully submit that the original specification supports the foregoing elements, in order to expedite prosecution of this application, the foregoing elements have been cancelled from claim 4. Accordingly, it is respectfully submitted that the pending objection has been overcome.

III. The Rejection Of The Claims Under 35 U.S.C. § 102

Claims 1, 4, 7, 12 and 13 were rejected under 35 U.S.C. § 102 as being anticipated by USP No. 5,399,518 to Sim. For the following reasons, Applicants respectfully submit that the pending claims are patentable over Sim.

Referring, for example, to Fig. 5 of the specification, claim 1 of the present invention recites a semiconductor device comprising:

1) a substrate 1 having a semiconductor region;

2) a first insulating film 16 formed on the semiconductor region 1 having a property of reflowing due to heat treatment under predetermined conditions;

3) a second insulating film 23x formed over the first insulating film 16 and containing at least silicon nitride, and

4) a supporting film 17 formed between the first and second insulating films 16 and 23x for applying to the insulating film 23x a stress against deformation of the second insulating film 23x caused by the heat treatment;

5) wherein the entire lower surface of the supporting film 17 contacts the upper surface of the first insulating film.

Furthermore, in the given embodiment, the first insulating film 16 is a BPSG film, the second insulating film 23x is an oxidized silicon nitride film and the supporting film 17 is a silicon oxide film.

Turning to Sim and referring to Fig. 35 thereof, Sim discloses a device comprising:

1) a substrate 10;

2) a gate electrode 18 formed over the substrate 10,

3) an insulating layer 19 formed over the substrate containing the gate electrode 18;

4) a planarization layer 22 formed on the insulating layer 19;

5) an etching stop layer 42 formed on the planarization layer 22; and

6) a dielectric film 110 formed on a storage electrode 100.

Furthermore, the insulating layer 19 of Sim is a pure oxide layer such as a high temperature oxide (HTO) layer; the planarization layer 22 comprises an insulating material such as BPSG or PSG; the etching stop layer 42 is made of silicon nitride and the dielectric film 110 is an oxide/nitride/oxide film or a Ta_2O_5 film (*see*, Sim, col. 6, lines 17-59 and col. 8, lines 3-15).

Turning to the pending rejection, it is asserted that the planarization layer 22 of

Sim corresponds to the claimed supporting film of the present invention. It is respectfully submitted that this conclusion is in error. More specifically, because the planarization layer 22 of Sim is an insulating layer, comprising BPSG or PSG, the layer 22 is subject to reflow during subsequent heating processes. As such, the planarization layer 22 of Sim cannot function as a supporting film for "applying to said second insulating film a stress against deformation of said second insulating film caused by the heat treatment". Thus, as layer 22 of Sim does not provide support to a second insulating film during a heat treatment (because layer 22 is in a reflow state), layer 22 does not correspond to the claimed supporting film.

Further, it is also asserted that the dielectric film 110 of Sim corresponds to the claimed second insulating film. This conclusion is also in error. The dielectric film 110 of Sim is deposited on the storage electrode 100. It does not appear that the alleged support layer 22 of Sim even contacts the dielectric film 110. As such, even assuming *arguendo* that the alleged support layer 22 of Sim was not subject to reflow, as the dielectric film 110 is not in contact with layer 22, layer 22 does not function to apply a stress against deformation to the dielectric film 110 during a heat treatment.

Finally, it is also asserted that the insulating layer 19 of Sim corresponds to the first insulating film 16 of the present invention. It is also respectfully submitted that this conclusion is in error. More specifically, the insulating layer 19 of Sim is a pure oxide layer, such as a high temperature oxide (HTO) layer, and the pure oxide does not have the property of reflow due to a heat treatment. Thus, layer 19 of Sim cannot correspond to the claimed first insulating layer which has the property of reflowing due to a heat treatment under predetermined conditions.

Thus, as anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, ***Kalman v. Kimberly-Clark Corp.***, 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983), and Sim fails to disclose at least the foregoing elements of the present invention, it is clear that Sim does not anticipate claim 1, or any claim dependent thereon.

For the foregoing reasons, it is respectfully submitted that claim 1, and all claims dependent thereon, are patentable over Sim.

IV. All Dependent Claims Are Allowable Because The Independent Claim From Which They Depend Is Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, ***Hartness International Inc. v. Simplimatic Engineering Co.***, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 1 is patentable for the reasons set forth above, it is respectfully submitted that all pending dependent claims are also in condition for allowance.

V. Request For Notice Of Allowance

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: 12/12/02

By: _____

Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W. , Suite 1200
Washington, D.C. 20005-3096
Telephone: 202-756-8000
Facsimile: 202-756-8087

WDC99 681558-1.043889.0929

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please cancel claim 34, without prejudice.

Please amend claim 4 and add new claims 37 and 38 as follows:

4. (Twice Amended) A semiconductor device as set forth in Claim 1, wherein said semiconductor device is a stacked DRAM cell comprising [a gate formed on said semiconductor region, an impurity diffusion layer formed in a region sideways of said gate in said semiconductor region,] an interlayer insulating film formed on [said gate and] said semiconductor region, a storage node filling an opening formed in said interlayer insulating film and extending over a part of said interlayer insulating film, a capacitor insulating film formed for coverage over said storage node and said interlayer insulating film, and a plate electrode formed in opposed relation with said storage node via said capacitor insulating film,

said first insulating film defining said interlayer insulating film,

said second insulating film defining said capacitor insulating film,

said supporting film is interposed between said interlayer insulating film and said capacitor insulating film.

Please add new claims 37 and 38 as follows:

--37. (New) A semiconductor device as set forth in claim 1, wherein said supporting film does not reflow due to said heat treatment which causes said first insulating film to reflow.

38. (New) A semiconductor device as set forth in claim 4, where said second insulating film is formed directly on the surface of said supporting film.--